Amendments to the Specification:

Please replace the original paragraphs identified below with the following amended paragraphs. In the amended paragraphs, inserted text is marked with underline, deleted text is marked with ~~strikethrough~~, and changes are identified by a vertical bar in the margin.

Please **delete** paragraph 16 at page 4 (Summary of the Invention) and **replace** it with new text as follows:

[16] The present invention describes techniques for memory access in which write operations to a memory including a re-programmable non-volatile memory are detected, if an address of the write operation from a processor logic indicates a first address area of the non-volatile memory, then performs a first write operation of data to said non-volatile memory. If the address of the write operation from the processor logic indicates a second address area of the non-volatile memory, then a second write operation of data is performed to the non-volatile memory according to a write operation speed that is different from the first write operation speed.

Please **amend** paragraph 19 at page 4 (Brief Description of Drawings) as follows:

[19] The present invention can be appreciated by the description which follows in conjunction with the following figures, wherein:

Fig. 1 shows a generalized block diagram of a system incorporating data processing aspects of the present invention;

Fig. 2 represents an illustrative embodiment of a data processing unit in accordance with the present invention;

Fig. 3 shows an illustrative embodiment of memory access in accordance with the present invention;

Fig. 3A ~~illustrate~~ illustrates a memory mapping according to an aspect of the invention as embodied in Fig. 3;

Fig. 3B illustrates a memory mapping translation operation according to an aspect of the invention;

Fig. 4 shows a memory map exemplar according to an aspect of the invention as embodied in Fig. 3;

Fig. 4A is a graphic illustration of the mapping process;

Figs. 5, 5A, and 6 show an embodiment of a read access operation in accordance with the present invention;

Figs. 7 and 7A show an embodiment of a write access operation in accordance with the present invention;

Figs. 8 - 13 show an illustrative embodiment of a caching mechanism in accordance with the present invention;

Figs. 14 and 15 illustrate an embodiment of a write operation in accordance with the present invention;

Figs. 16 and 17 show additional aspects of the write operation of the present invention; and

Fig. 18 is a schematic representation of a typical re-programmable, non-volatile memory cell.